CLAIMS

WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a first wafer including a silicon germanium layer, a strained silicon layer, and a first insulating layer; and

a second wafer including a substrate and a second insulating layer, the second insulating layer being attached to the first insulating layer.

2. The integrated circuit of claim 1, wherein the substrate is a bulk semiconductor substrate.

3. The integrated circuit of claim 2, wherein the silicon germanium layer includes a hydrogen breaking interface.

4. The integrated circuit of claim 1, wherein a channel region is disposed in the strained silicon layer.

5. The integrated circuit of claim 4, wherein a source region and a drain region are disposed in the strained silicon layer.

6. The integrated circuit of claim 5, wherein an aperture is formed in the silicon germanium layer to expose the strained silicon layer.

7. The integrated circuit of claim 6, wherein a gate structure is provided in the aperture.

8. A multilayer structure containing a plurality of SMOS transistors, the multilayer structure comprising:

a semiconductor/germanium layer;

a strained semiconductor layer including a source and a drain provided below the semiconductor/germanium layer, the semiconductor/germanium layer having an aperture;

a gate dielectric above the strained semiconductor layer and within the aperture; and

a gate conductor within the aperture.

9. The multilayer structure of claim 8, further comprising:

a spacer in the aperture separating the semiconductor/germanium layer and the gate conductor.

10. The multilayer structure of claim 8, further comprising:

a silicide layer disposed above the semiconductor/germanium layer.

11. A method of making an SMOS structure containing a plurality of transistors, the method comprising:

providing a first semiconductor substrate including a base layer, a strained semiconductor layer, and a first oxide layer;

attaching a second semiconductor substrate including a second oxide layer to the first oxide layer; and

separating the base layer from the first substrate.

12. The method of claim 11, wherein a semiconductor/germanium layer is above the strained semiconductor layer.

13. The method of claim 12, further comprising:

providing an aperture in the semiconductor/germanium layer.

14. The method of claim 13, further comprising:

doping the strained semiconductor layer through the aperture.

15. The method of claim 15, wherein the doping step forms source and drain extensions.

16. The method of claim 13, further comprising:

providing a gate conductor in the aperture.

17. The method of claim 16, further comprising:

separating the gate conductor from the silicon/germanium layer with a spacer material.

18. The method of claim 12, further comprising:

siliciding the semiconductor/germanium layer.

19. The method of claim 11, wherein the attaching step is a hydrogen bonding step.